C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02RSM1
NAME – Research Methodology (RSM)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02RSM1	Research Methodology(RSM)	02	00	00	02	02	30	1.5	70	3.0	---	---	---	100

Objectives:-

- The objective of the course is to introduce the basic methods of conducting research, explore ideas in formulating research objectives and hypotheses and sample framework for taking up research studies in a structured manner.
- Also it is intended to facilitate for the development of an insight into different statistical tools for data analysis, interpretation and presentation of reports in different areas of research.

Prerequisites:-Knowledge of Basic research methods studied in B.E.

Course Outlines:-

Sr. No.	Course Contents
1	**Introduction**: Meaning of Research, objectives of Research ,Types of research, Various Steps in Research process, Types of Research, Research Approaches, Significance of Research
2	**Problem formulation**: Review of Research Literature: Purpose and use of literature review, locating relevant information, use of library & electronic databases, preparation & presentation of literature review, research article reviews, theoretical models and frame work. Identification of gaps in research, formulation of research problem, definition of research objectives.
3	**Research Design**: Qualitative Methods: Types of hypothesis and characterization. Quantitative Methods: Statistical methods for testing and evaluation. Characterization of experiments: Accuracy, reliability, reproducibility, sensitivity, Documentation of ongoing research.
4	**Research Publication & Presentation**: Structure and Components of thesis and reports, formatting issues, citation methods, references, effective oral presentation of research. Quality indices of research publication
5	**Research Ethics and Morals:** Issues related to plagiarism, collaborative models and ethics, acknowledgements. Intellectual Property Rights: copy rights, copy left: patents, Industrial designs, Trademarks.

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Learning Outcomes:-

- Students successfully completing the Master degree have an understanding of the content, methods, theories, and professional ethics associated with research methodology.
- Research Methodology as a subject should help researchers to prepare the literature in chronological pattern and should logically analyze the concerns.
- This subject should help in framing the research problems to enhance the scale of understanding.
- This subject should help researchers to use tools, techniques, concepts and worlds best practices to present a unique research.
- Acquisition of skills for developing a research proposal for a master thesis project

Books Recommended:-

1. Research Methodology (Methods and Techniques), **Kothari, C.R**., New Age Publisher
2. Research Methods- A Process of Inquiry, **Graziano, A.M., Raulin, M.L**, Pearson Publications, 7th Edition, 2009.
3. How to Write a Thesis,**Murray, R**. Tata McGraw Hill, 2nd Edition, 2010.
4. Writing For Academic Journals, **Murray, R**., McGraw Hill International, 2009.
5. Writing for Publication, **Henson, K.T.**, Allyn&Bacon, 2005.

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02AVD1
NAME – Analog VLSI Design (AVD)

Teaching & Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02AVD1	Analog VLSI Design (AVD)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives:-

- The primary objective of this subject is to introduce about real implementation of analog circuits.
- Involve students in practical studies of linear and non-linear analog circuits and special purpose CMOS designs.

Prerequisites: -Detailed knowledge of Analog and Digital Electronics and Basics of VLSI back-end tools such as LTSpice and Microwind is necessary. Basic knowledge of Circuit Theory is essential.

Course Outlines:-

Sr. No.	Course Contents
1	**Current Mirror:** The Basic Current Mirror, Matching Currents in the Mirror, Biasing the Current Mirror, Cascoding the Current Mirror, The Simple Cascode -DC Operation, Low-Voltage (Wide-Swing) Cascode, Wide-Swing Cascode, Biasing Circuits .
2	**Differential Amplifiers:** The Source-Coupled Pair, The Source Cross-Coupled Pair, Cascode Loads (The Telescopic Diff-Amp), Wide-Swing Differential Amplifiers, Current Differential Amplifier, Constant Transconductance Diff-Amp.
3	**Nonlinear Analog Circuits:** Basic CMOS Comparator Design, Preamplification, Decision Circuit, Output Buffer, Characterizing the Comparator, Comparator DC Performance, Clocked Comparators, Input Buffers Revisited, Adaptive Biasing.
4	**Special Purpose CMOS Circuits:** The Schmitt Trigger, Multivibrator Circuits, The Monostable Multivibrator, The Astable Multivibrator, Input Buffers, Skew in Logic Gates, Differential Circuits, Charge Pumps (Voltage Generators), Using MOSFETs for the Capacitors, Generating Higher Voltages: The Dickson Charge Pump, Clock Driver with a Pumped Output Voltage, NMOS Clock Driver
5	**Phase Locked Loops:** PLL – simple PLL, Phase detector, Dynamics of Simple PLL, Non-ideal effects in PLL, Charge-pump PLL, Delay Locked Loops, Applications of PLL.

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Learning Outcomes:-

- Students to identify the real architecture of analog circuits.
- At the end of this course students will gain hands-on experience on back-end design of analog CMOS circuits using back-end simulation tools.

Books Recommended:-

1. CMOS Circuit Design, Layout, and Simulation, **R. Jacob Baker**, Willy, IEEE Press,3rd Edition.
2. Analog Integrated Circuit Design, **David. A. Johns and Ken Martin**, John Wiley and Sons, 2001.
3. Design of Analog CMOS Integrated Circuit, **Behzad Razavi**, Tata McGraw HILL, 2002.
4. CMOS Analog Circuit Design, **Philip Allen & Douglas Holberg**, Oxford University Press, 2002.

Research Reference:-

1. http://www.ti.com/lit/ds/sprs030a/sprs030a.pdf
2. http://www.ti.com/lit/ds/sprs039c/sprs039c.pdf
3. http://www.ti.com/lit/ds/symlink/tms320c6713.pdf

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02AES1
NAME – Advanced Embedded Systems (AES)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
							Sessional Exam		University Exam		Internal		University	
		Th	Tu	Pr	To		Marks	Hours	Marks	Hours	Pr	TW	Pr	
5TE02AES1	Advanced Embedded Systems (AES)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge on advanced design concepts of embedded systems such as embedded hardware, software, memory, hardware/software co-design, multiprocessor systems etc.

Prerequisites: Basic knowledge of embedded systems, digital hardware and software is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction to Embedded Hardware and Software:** Introduction, Combinational and Sequential Logic, Custom Single-Purpose Processor Design, RT-Level Custom Single-Purpose Processor Design, Optimizing Custom Single-Purpose Processors, Basic Architecture and Operation of Software, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIP's), Selecting a Microprocessor, General-Purpose Processor Design
2	**Memory:** Introduction, Memory-Write Ability and Storage Permanence, Common Memory Types, Composing Memories, Memory Hierarchy and Cache, Advanced RAM
3	**State Machine and Concurrent Process Models:** Introduction, Models vs. Languages, Text vs. Graphics, A Basic State Machine Model: Finite-State Machines (FSM), Using State Machines, Hierarchical/Concurrent State Machine Model (HCFSM) and the State charts Language, Program-State Machine Model (PSM), Concurrent Process Model, Concurrent Processes, Communication and Synchronization among Processes, Implementation, Dataflow Model, Real-Time Systems
4	**Multiprocessors:** Why Multiprocessors? , CPU and Accelerators, Multiprocessor Performance Analysis, Consumer Electronics Architecture, Design Examples: Cell Phones, Compact Discs and DVDs, Audio Players, Digital Still Camera, Video Accelerator,
5	**Design Technology:** Introduction, Automation: Synthesis, Verification: Hardware/Software Co-Simulation, Reuse: Intellectual Property (IP) Cores, Design Process Models

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Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the advanced embedded hardware and software.
- Understand different types of memory used in embedded systems.
- Understand state-machine concept and its application in embedded system design and verification.
- Understand basics of multiprocessor embedded systems.

Books Recommended:-

1. Embedded System Design: A Unified Hardware/Software Introduction, **Frank Vahid and Tony Givargis**, Wiley
2. Computers as Components – Principles of Embedded Computing System Design, **Wayne Wolf**, Morgan Kaufmann Publishers
3. An Embedded Software Primer, **David E, Simon**, Pearson Education
4. Embedded System Design, **Steve Heath**, Elsevier

C.U.SHAH UNIVERSITY – WADHWANCITY

FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02WTE1
NAME – Wireless Technology for Embedded Systems (WTE)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02WTE1	Wireless Technology for Embedded Systems (WTE)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide fundamental knowledge of wireless technologies used in embedded system design and biggest application of wireless technology in embedded system architecture – Wireless Sensor Networks.

Prerequisites: Basic knowledge of Computer Networking and Protocols is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction to Wireless Technologies:** History, Frequency Spectrum, Signal Propagation and Degradation, Serial and Parallel Communication, Asynchronous and Synchronous Transmission, Duplexing Techniques, Multiplexing and Multiple Access Methods, Spread Spectrum Technology
2	**Introduction to Wireless Sensor Networks (WSNs):** Types and Examples of WSN, Challenges for WSNs, Why are sensor networks different?
3	**Single Node Architecture:** Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environment
4	**Network Architecture:** Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design Principles for WSNs, Service Interfaces of WSNs, Gateway Concepts
5	**WSN Communication Protocols – Physical Layer:** Wireless Channel and Communication Fundamentals, Physical Layer and Transceiver Design Considerations in WSNs
6	**MAC Protocols:** Fundamentals of Wireless MAC Protocols, Low Duty-Cycle Protocols and Wake-up Concepts, Contention-based Protocols, Schedule-based Protocols, IEEE 802.15.4 MAC Protocol
7	**Link Layer Protocols:** Fundamentals, Error Control, Framing, Link Management
8	**Time Synchronization:**

	Introduction to Time Synchronization Problem, Protocols based on Sender/Receiver Synchronization, Protocols based on Receiver/Receiver Synchronization
9	**Localization and Positioning:** Properties, Possible Approaches, Mathematical Basics for Lateration Problem, Single-hop Localization, Positioning in Multi-hop Environment
10	**Routing Protocols:** Gossiping and Agent-based Unicast Forwarding, Energy Efficient Unicast, Broadcast and Multicast, Geographic Routing, Mobile Nodes
11	**Data-Centric and Content-based Networking:** Introduction, Data-Centric Routing, Data Aggregation, Data-Centric Storage

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand wireless technology fundamentals.
- Understand basics of wireless sensor network and its use in embedded system networking and design.

Books Recommended:-

1. Bluetooth Technology, **C. S. R. Prabhu and A. Prathap Reddi**, PHI
2. Protocols and Architectures for Wireless Sensor Networks, **Holger Karl and Andreas Willig**, Wiley
3. Fundamentals of Sensor Network Programming – Applications and Technology, **S. Sitharama Iyengar, Nandan Parameshwaran, Vir V. Phoha, N. Balakrishnan, Chuka D. Okoye**, Wiley

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02VDA1
NAME – VLSI Design Automation (VDA)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02VDA1	VLSI Design Automation (VDA)	04	00	02	06	05	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge of VLSI physical design, Different algorithms for Floorplanning, channel routing, partitioning and placement, with complete knowledge of layout generation.

Prerequisites: Basic knowledge of Digital Electronics and CMOS VLSI Design is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**VLSI Physical Design Automation:** VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Comparison of Different Design Styles.
2	**Design and Fabrication of VLSI Devices:** Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices, Inverters, NAND and NOR Gates, Memory Cells.
3	**Basic Data Structures and Basic Algorithms:** Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures
4	**Partitioning:** Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning.
5	**Floorplanning:** Classification of Floorplanning Algorithms, Constraint Based Floorplanning, Integer Programming Based Floorplanning, Rectangular Dualization, Hierarchical Tree Based Methods, Floor planning Algorithms for Mixed Block and Cell Designs, Simulated Evolution Algorithms, Timing Driven Floorplanning, Theoretical advancements in Floorplanning, Chip planning, Pin Assignment.
6	**Placement:** Classification of Placement Algorithms, Simulation Based Placement Algorithms, Comparison of Simulation Based Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement.
7	**Global Routing:** Problem Formulation, Classification of Global Routing Algorithms, Maze Routing

	Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms, Integer Programming Based Approach, Performance Driven Routing.
8	**Layout generation:** Introduction, Layout generation, Standard-cell Generation, Optimization of Gate-Matrix Layout, Programmable Logic Arrays

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of Physical design of Integrated Circuits.
- Understand different Algorithms of Data Structure, Floorplaning, Routing and Placement.
- Understand complete Layout generation of Digital Logic with Different VLSI Design Style.

Books Recommended:-

1. Algorithms for VLSI Physical Design Automation, **Naveed A. Sherwani**,(Intel Corporation) Kluwer Academic Publishers, Third Edition.
2. VLSI Physical Design Automation - Theory and Practice, **Sadiq M Sait**, **Habib Youssef** World Scientific Publishing Co. Pvt. Ltd.
3. Algorithms for VLSI Design Automation, **Sabih H. Gerez**, John Wiley & Sons.

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - II **CODE**: -5TE02MSS1
NAME – Mixed Signal System Design (MSS)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02MSS1	Mixed Signal System Design (MSS)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- In this course, student will study static & dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, and layout and design rules, stick diagrams. At the end of the course the student will know mixed signal designs like DAC, ADC, etc.

Prerequisites: Students enrolled in this course are expected to have an undergraduate-level equivalent background in the following topics: Logic Circuit Design, Microelectronics, MOSFET Operation, MOS-based Logic gates, Fundamental programming skills

Course Outlines: -

Sr. No.	Course Contents
1	**Data Converter Fundamentals:** Analog Versus Discrete Time Signals, Converting Analog Signals to Digital Signals, Sample-and-Hold (S/H) Characteristics, Digital-to-Analog Converter (DAC) Specifications-Differential Nonlinearity-Integral Nonlinearity etc., Analog-to-Digital Converter (ADC) Specifications-Quantization Error-DNL-INL-Missing Codes-Signal-to-Noise Ratio etc.
2	**DAC Architectures:** Digital Input Code, Resistor String DAC, R-2R Ladder Networks, Current Steering DAC, Charge-Scaling DACs, Binary-Weighted, Capacitor Array, The Split Array, Cyclic DAC, Pipeline DAC
3	**ADC Architectures:** Flash ADC, The Two-Step Flash ADC, Accuracy Issues Related to Operational Amplifiers, The Pipeline ADC, Integrating ADCs, Single-Slope Architecture, Dual-Slope Architecture, The Successive Approximation ADC, The Charge-Redistribution Successive Approximation ADC, The Oversampling ADC, Differences in Nyquist Rate and Oversampled ADCs, The First-Order Delta-Sigma Modulator, The Higher Order Delta-Sigma Modulators
4	**Memory Circuits:** Array Architectures, Sensing Basics, NMOS Sense Amplifier (NSA), The Open Array Architecture, PMOS Sense Amplifier (PSA),The Folded, Peripheral Circuits, Sense Amplifier Design, Kickback Noise and Clock Feedthrough, Row/Column Decoders, Global and Local Decoders, Row Drivers, Memory Cells, The SRAM Cell, Read-Only Memory (ROM), Flash Memory.

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Learning Outcomes: -

- Be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
- Be able to create models of moderately sized CMOS circuits that realize specified digital functions.
- Be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
- Have an understanding of the characteristics of CMOS circuit construction and the comparison between different state-of-the-art CMOS technologies.

Books Recommended:-

1. CMOS Circuit Design, Layout, and Simulation, **R. Jacob Baker**, Willy, IEEE Press,3rd Edition.
2. Integrated A-D and D-A Converters, **Plassche, Rudy J.Van De**, Springer (2007)2nd ed.
3. Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, **Jespers, P.G.A.**, Oxford University Press (2001).

Research Reference:-

1. International Journal of Advanced Research in Computer Science and Electronics Engineering (IJARCSEE),ISSN: 2277 – 9043
2. Applicable Algebra in Engineering, Communication and Computing, ISSN: 0938-1279, 1432-0622
3. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions
4. Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions
5. Very Large Scale Integration (VLSI) Systems, IEEE Transactions

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: - Electronics & Communication Engineering
SEMESTER: - II **CODE**: -5TE02FAA1
NAME – FPGA Architecture and Applications (FAA)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02FAA1	FPGA Architecture and Applications (FAA)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- This is an advanced graduate class on programmable logic.
- The course will cover different FPGA families and its basic architecture.

Perquisites: The course requires deep knowledge of digital electronics and hardware descriptive language.

Course Outlines: -

Sr. No.	Course Contents
1	**Programmable logic Devices:** ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming. Applications and Implementation of MSI circuits using Programmable logic Devices.
2	**FPGAs:** Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs, Introduction to advanced FPGAs: Xilinx Virtex and ALTERA Stratix
3	**Finite State Machines (FSM) for FPGA:** Top Down Design, State Transition Table, State assignments for FPGAs, realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine. **FSM Architectures:** Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.
4	**System Level Design:** Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs. **Case studies:** Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

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Learning Outcomes: -

- Upon completion of this course, students should be able to program different logics on FPGA using Xilinx ISE.

Books Recommended:-

1. Field Programmable Gate Array Technology, **S. Trimberger, Edr**, 1994, Kluwer Academic Publications.
2. Engineering Digital Design, **Richard F.Tinder**, 2nd Edition, Academic press.
3. Fundamentals of logic design, **Charles H. Roth**, 4th Edition Jaico Publishing House.

Research References:-

1. Parallel and Distributed Systems, IEEE Transactions on
2. Communications, IEEE Transactions on
3. Wireless Communications, IEEE Transactions on

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02SDP1
NAME – System Design with Advanced Processors (SDP)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02SDP1	System Design with Advanced Processors (SDP)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge of advanced processors such as ARM Cortex-M0 and DSP Processors and their applications in embedded system design.

Prerequisites: Basic knowledge of ARM architecture, assembly and C programming, and Digital Signal Processing is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction to ARM Cortex-M0 Processor:** Background of ARM Processors, ARM Cortex-M0 Processor Features and Advantages
2	**Architecture of ARM Cortex-M0 Processor:** Overview, Programmer's Model, Memory System Overview, Stack Memory Operations, Exception and Interrupts, Nested Vectored Interrupt Controller (NVIC), System Control Block (SCB), Program Image and Startup Sequence
3	**Cortex-M0 Programming:** Inputs and Outputs, Development Flow, C and Assembly Programming, What is in a Program Image? , C Data Types, Accessing Peripherals in C, Cortex Microcontroller Software Interface Standard (CMSIS)
4	**Instruction Set and Examples:** Background of ARM and Thumb Instruction Set, Assembly Basics, Instructions and Examples, Pseudo Instructions, Program Control, Data Access, Data Type Conversion, Data Processing
5	**Memory System:** Memory Map, Program Memory, Boot Loader and Memory Remapping, Data Memory, Little Endian and Big Endian Support, Memory Attributes
6	**Exception and Interrupts:** Exception Types on Cortex-M0 Processor, Exception Priority Definition, Vector Table, Exception Sequence Overview, EXC_RETURN, Details of Exception Entry and Exception Exit Sequence
7	**Interrupt Control and System Control:** Overview of NVIC and SCB Features, Interrupt Enable and Clear Enable, Interrupt

	Pending and Clear Pending, Interrupt Priority Level, Generic Assembly Code for Interrupt Control, Exception Masking Register, Interrupt Inputs and Pending Behavior, Interrupt Latency, Control Registers for System Exceptions, System Control Registers
8	**Cortex-M0 Products:** Overview, Microcontroller Products and Application-Specific Standard, Products (ASSPs) – NXP Cortex-M0, NuMicro Family, Mocha-1 ARM Cortex-M0 Configurable Array, Melfas MCS-7000 Series Touch Screen Controllers
9	**Architecture for Programmable Digital Signal Processing Devices:** Introduction, Basic Architectural Features, Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing
10	**Programmable Digital Signal Processors:** Introduction, Commercial Digital Signal Processing Devices, The Architecture of TMS320C54xx Digital Signal Processors, Addressing Modes of the TMS320C54xx Processors, Memory Spaces of TMS320C54xx Processors, Program Control, TMS320C54xx Instructions and Programming, On-Chip Peripherals, Interrupts, Pipeline Operation of the TMS320C54xx Processors

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of ARM Cortex-M0 processor.
- Understand programming and interfacing of ARM Cortex-M0 processor.
- Understand programming and interfacing of DSP processors.

Books Recommended:-

1. The Definitive Guide to the ARM Cortex-M0, **Joseph Yiu**, Newnes
2. Digital Signal Processing Implementations – Using DSP Mircoprocessors, **Avtar Singh, S. Srinivasan**, Thomson/Brooks/Cole
3. Embedded/Real-Time Systems – Concepts, Design & Programming, **Dr. K. K. V. Prasad**, Dreamtech Press

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FACULTY OF: - Technology & Engineering
DEPARTMENT OF: -Electronics & Communication Engineering
SEMESTER: - II **CODE**: - 5TE02RKS1
NAME – RTOS Kernel and System Drivers (RKS)

Teaching &Evaluation Scheme:-

Subject Code	Subject Name	Teaching Schemes (Hours)				Credits	Evaluation Schemes							
							Theory				Practical (Marks)			Total
											Internal		University	
		Th	Tu	Pr	To		Sessional Exam		University Exam		Pr	TW	Pr	
							Marks	Hours	Marks	Hours				
5TE02RKS1	RTOS Kernel and System Drivers (RKS)	03	00	02	05	04	30	1.5	70	3.0	---	20	30	150

Objectives: -

- The objective of the subject is to provide detailed knowledge on Real-Time Operating Systems, its architecture, functions and design.

Prerequisites: Basic knowledge of operating systems and embedded hardware and software is necessary.

Course Outlines: -

Sr. No.	Course Contents
1	**Introduction and Basics of Developing for Embedded Systems:** Real Time Embedded Systems, Overview of Linkers and Linking Process, Executable and Linking Format, Mapping Executable Images into Target Embedded Systems
2	**Embedded System Initialization:** Target System Tools and Image Transfer, Target Boot Scenarios, Target System Software Initialization Sequence, On-Chip Debugging
3	**Introduction to Real-Time Operating Systems (RTOS):** History and Definition of an RTOS, Scheduler, Objects, Services, Key Characteristics of an RTOS
4	**Tasks and Semaphore:** Defining a Task, Task States and Scheduling, Typical Task Operation and Structure, Synchronization, Communication and Concurrency, Defining Semaphores, Typical Semaphore Operation and Use
5	**Message Queues and Other Kernel Objects:** Defining Message Queues, Message Queue States and Contents, Message Queue Storage, Typical Message Queue Operation and Use, Pipes, Event Registers, Signals, Condition Variables
6	**Other RTOS Services:** Other Building Blocks, Component Configuration
7	**Exceptions and Interrupts:** What are Exceptions and Interrupts? , Applications of Exceptions and Interrupts, A Closer Look, Processing General Exceptions, Nature of Spurious Interrupts,
8	**Timer and Timer Services:** Real-Time Clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routine, A Model for Implementing the Soft-Timer Handling

	Facility, Timing Wheels, Soft Timers and Timer related Operations
9	**I/O Subsystems:** Basic I/O Concepts, I/O Subsystem
10	**Memory Management:** Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory Management, Blocking vs. Non-blocking Memory Functions, Hardware Memory Management Unit
11	**Synchronization and Communication:** Synchronization, Communication, Resource Synchronization Methods, Critical Section Revisited, Common Practical Design Patterns, Specific Solution Design Patterns
12	**Device Drivers:** Device Drivers for Interrupt Handling, Memory Device Drivers, On-board Bus Device Drivers
13	**Case Studies of RTOS:** µCOS-II, VxWorks, Windows CE, RTLinux

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the basics of Real-Time Operating Systems.
- Understand architecture, functions and design of an RTOS.
- Understand device drivers and examples of RTOSes.

Books Recommended:-

1. Real Time Concepts for Embedded Systems, **Qing Li and Carolyn Yao**, CMP Books
2. Embedded System Architecture – A Comprehensive Guide for Engineers and Programmers, **Tammy Noergaard**, Newnes
3. Embedded Systems – Architecture, Programming and Design, **Raj Kamal**, McGraw Hill